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Lamination Method for the Study of Interfaces in Polymeric Thin Film Transistors

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Semiconducting polymers are important materials for large area electronics because they offer the opportunity to greatly reduce the cost of fabrication of displays, electric paper, and imagers.[1] Processing methods that do not chemically or mechanically damage organic films are important to enable detailed study of the electrical properties of organic thin film transistors (OTFTs), in particular the interface between the gate dielectric and the semiconducting film.[2] We present here a method to laminate polymeric semiconducting films using an elastomeric support made with poly(dimethylsiloxane), PDMS (Figure 1). This process enables the direct examination of the effect of the interface of a semiconducting polymer and a gate dielectric on the electrical performance of OTFTs.

Techniques to laminate semiconducting polymeric films have been used previously to fabricate photovoltaics and light emitting diodes. For example, a polymeric film can be "floated" off of a substrate by immersion into a water bath.[3] The film is then carefully manipulated, placed onto the final substrate, and then annealed to drive off any residual water. Polymeric supporting layers have been used to laminate films at relatively low temperatures (60 °C) and moderate pressures.[4] These techniques have enabled the study of interfacial interactions but are hindered by the fragility of free-standing films and the need for thermal annealing and pressure to ensure contact between laminated layers.

Recently, compliant PDMS stamps have been used to fabricate OTFTs. OTFTs have been fabricated by laminating metallic contacts supported by a PDMS stamp onto molecular semiconductors.[5] PDMS has also been used as a gate dielectric to make contact to single-crystal OTFTs.[6] Poly(3-hexylthiophene), P3HT, has been spun directly on PDMS and transferred to a substrate to form TFTs with mobilities of 0.007 $cm^2/(V\ s)$.[7]

The lamination scheme used here is outlined in Figure 1. First, a film of a semiconducting polymer is spun onto a silicon wafer that has been coated with a self-assembled monolayer of an alkyltrichlorosilane. Typically, we anneal the semiconducting film to remove any excess solvent and to improve its electrical properties.[8] Second, a flat stamp of PDMS (∼1−5 mm thick) is placed onto the dry semiconducting film (∼50−100 nm thick) and peeled away. Last, the film, now mechanically supported by the PDMS stamp, is placed into contact with a coplanar electrode structure to fabricate a thin-film transistor. We have fabricated OTFTs using this method with a number of materials including poly[5,5′-bis(3-dodecyl-2-thienyl)-2,2′-bithiophene], or PQT-12,[8] and P3HT. [9]

The success of the delamination step depends on the difference in adhesion between the semiconducting film and the substrate and between the film and the PDMS stamp. Films spun onto plasma-cleaned substrates cannot be easily delaminated by a PDMS stamp. Coating the initial substrate with a self-assembled monolayer (SAM) lowers its surface energy sufficiently to allow the film to be peeled from the substrate by PDMS (the water contact angle on the SAM is ∼110°, while that on PDMS is ∼85°). The use of PDMS is preferable to an adhesive tape because it can be readily fabricated into a sheet with low surface roughness using silicon wafers, it is electrically insulating, and its mechanical properties allow the supported film to conform to the electrode structure at room temperature.

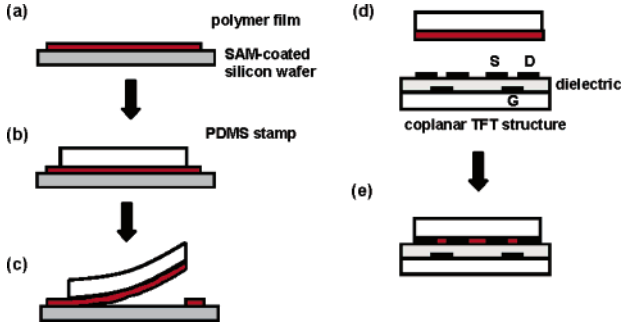

Figure 1. Schematic of the lamination process. (a) A film of a semiconducting polymer is spin-coated onto a silicon wafer that has been coated with a self-assembled monolayer formed from octyltrichlorosilane (OTS). (b) A PDMS stamp is placed into contact with the film of the semiconducting polymer. (c) The PDMS stamp is carefully peeled from the substrate. (d) A coplanar TFT structure comprising source (S) and drain (D) contacts (Au 100 nm thick with a 6 nm Cr adhesion layer), a gate dielectric of silicon dioxide on silicon nitride ($C = 30$ nF/cm^2), and a chromium gate (G) contact (100 nm thick) is fabricated on a glass wafer. (e) The supported semiconducting film is placed into contact with a coplanar TFT structure to form the finished TFT.

It is important to examine the low voltage behavior of TFTs to determine whether good electrical contact is being made between the source and the semiconducting film. The current−voltage, $I-V$, characteristics of TFTs made with PQT-12 and P3HT are shown in Figure 2. For PQT-12 films laminated onto dielectric surfaces with OTS, we obtained mobilities, μ, of 0.03 $cm^2/(V\ s)$ and threshold voltages, V_T, ranging from 0 to −2 V. For comparison, TFTs fabricated with P3HT had $\mu = 0.005$ $cm^2/(V\ s)$ and $V_T = 0$ to −1 V. The mobilities of TFTs with both polymers varied by ∼30% sample to sample. The films were not patterned and, therefore, show lower ratios of the on- to off-current (∼10^3) than are normally observed for high-quality TFTs of PQT-12 and P3HT. The leakage current arises from the polymer film that is in contact with the source and drain on the glass substrate; this material is ungated and, if lightly doped, can cause a leakage current. The leakage currents for P3HT and PQT-12 are small enough not to strongly affect the extraction of device parameters. The output characteristics of TFTs with relatively small channel lengths (10

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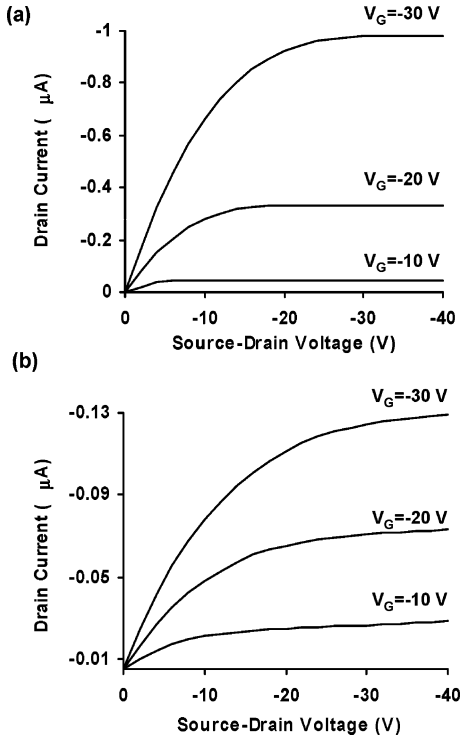

Figure 2. Output characteristics of laminated OTFTs with $W = 200$ μm and $L = 50$ μm: (a) PQT-12; (b) P3HT. The P3HT device does not exhibit perfect saturation due to the leakage current in the TFT.

μm) show the presence of a small, nearly ohmic contact resistance of $\sim$1 kΩ cm for PQT-12, which is similar to that obtained with devices fabricated by spin-coating.[10] The small value of the contact resistance suggests that the semiconductor is making good electrical and mechanical contact to the edge of the source electrode. The source and drain contacts from our fabrication process have a slight taper at the edge, which may have aided in achieving good contact.

It is important to compare the performance of the laminated devices to that of those fabricated by spin-coating. We spun PQT-12 films onto doped silicon wafers with thermal oxide layers and source and drain contacts and used a portion of the film for laminated OTFTs. The OTFTs on the oxide substrate had $\mu = 0.06$ cm^2/(V s), while those laminated from the transferred film had $\mu = 0.03$ cm^2/(V s). For TFTs made with P3HT, we obtained $\mu =$ 0.01 and 0.005 cm^2/(V s), respectively. While contact resistance is a likely explanation for the decrease in mobility upon lamination, the decrease was nearly a factor of 2 for both PQT-12 and P3HT. The two materials have similar contact resistances with gold electrodes but different average mobilities in our hands.[9,10] The observation of a contact resistance should be more pronounced for films with higher mobility, but the decrease in mobility is similar for both materials. A possible explanation is mechanical damage to the films as they are peeled from the substrate or laminated onto the electrodes. Upon a brief low-temperature anneal ($\sim$80 °C), the effective mobility of TFTs from both P3HT and PQT-12 films increased to their values on the initial substrate. The annealing step may eliminate defects in the film (e.g. microcracks from stress).

The use of laminated films enables the study of the effect of the dielectric surface on the effective mobility of TFTs. It has been observed that a gate dielectric with a hydrophobic surface produces a TFT with higher mobility than one with a hydrophilic surface using PQT-12 and other polymers.[2,9] It is not known whether this result is due to the structure of the semiconducting film at the interface or trapping at interfacial electronic states. Interestingly, laminated films of PQT-12 on bare oxide substrates showed the same mobility as those laminated onto surfaces coated with a SAM of OTS [$\mu = 0.03$ cm^2/(V s)]. In contrast, films spun on bare oxide dielectrics show $\mu = \sim 10^{-3}-10^{-4}$ cm^2/(V s) depending on the substrate. These results strongly suggest that the morphology of the film is maintained during the transfer step and the surface of the supported semiconducting film is not damaged during the lamination process. Furthermore, when the laminated PQT-12 films on these surfaces were annealed near 120 °C (the proposed side chain melting temperature),[8] the mobility of the TFTs decreased to 0.005 cm^2/(V s), suggesting that the film reorders due to specific interactions with the substrate. These results directly demonstrate that the lower mobility on bare silicon dioxide dielectric layers is not due to surface dipoles formed by the Si$-$OH groups and that it is likely due molecular ordering in the film.

The lamination method described here has advantages over previous methods because the films do not need to be exposed to a solvent for transfer, the process can be done at room temperature without pressure, and it enables good electrical contacts to be formed to the films. This method provides a new technique to study the effects of processing conditions on polymer films and should aid in the study of organic semiconductor$-$dielectric interfaces.[2,12]

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Supporting Information Available: Detailed information about the fabrication of the TFTs, optical micrographs of finished devices, atomic force micrographs, and $I-V$ data for TFTs. This material is available free of charge via the Internet at http://pubs.acs.org.

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